WHAT IS CLAIMED IS:

1. A computer system which includes a plurality of memory banks, comprising:

a processor unit which controls processing of an operation; and

additional processing units each of which corresponds to one of the memory banks and performs the operation independently of the processor unit, wherein the operation is performed about data stored in the corresponding memory bank based on an instruction or data provided from the processor unit.

2. The computer system of claim 1, wherein the operation that each of the additional processing units performs includes at least one of calculating the data, reading the data from the memory bank, or writing the data to the memory bank.

3. The computer system of claim 1, wherein the address of the data in the memory bank is provided by the processor unit, and each of the additional processing units reads the data by referring to the address and performs the operation designated by the processor about the read data, and writes the result of the process into the address.

4. The computer system of claim 3, wherein when the additional processing unit receives information from the processor unit and the operation designated by the processor is one of the four basic operations of arithmetic, the additional processing unit performs one of the four basic operations using the read data and the received information.

5. The computer system of claim 3 further comprising:

an addition updating unit which updates the data located in the address designated by the processor unit to a value resulting from adding of the data and a predetermined value; and

a subtraction updating unit which updates the date located in the address designated by the processor unit to a value resulting from subtracting a predetermined value from the data.

6. The computer system of claim 1, wherein the processor unit performs a vector operation.

7. The computer system of claim 1, wherein the processor unit consists of a plurality of processors each of which performs an operation in parallel with another processor.

8. A method of controlling computation in a computer system which includes a plurality of memory banks, comprising the steps of:

instructing, at a processor unit, additional processing units each of which is connected to one of the memory banks and works independent of the processor unit, to perform an operation;

reading, at the additional processing unit, data located in an address designated by the processor unit from the corresponding memory bank;

performing, at the additional processing unit, the operation instructed by the processor unit about the read data; and

writing, at the additional processing unit, the result of the operation into the address designated by the processor unit.

9. The method of claim 8 further comprising the step of receiving, at the additional processing unit, information from the processor unit, wherein the operation instructed by the instructing step is one of the four basic operations of arithmetic, and the performing step performs one of the four basic operations using the read data and the received information.

10. The method of claim 9 comprising the steps of:

updating the data located in the address designated by the processor unit to a value resulting from adding of the data and a

predetermined value; and

updating the date located in the address designated by the processor unit to a value resulting from subtracting a predetermined value from the data.

11. The method of claim 9, wherein the processor unit performs a vector operation.

12. The method of claim 9, wherein the processor unit consists of a plurality of processors each of which performs an operation process in parallel with another processor.

13. A recording medium readable by a computer, tangibly embodying a program of instructions executable by the computer to perform a method of controlling computation in a computer system which includes a plurality of memory banks, the method comprising the steps of:

instructing, at a processor unit, additional processing units each of which is connected to one of the memory banks and works independent of the processor unit, to perform an operation;

reading, at the additional processing unit, data located in an address designated by the processor unit from the corresponding memory bank;

performing, at the additional processing unit, the operation instructed by the processor unit about the read data; and

writing, at the additional processing unit, the result of the operation into the address designated by the processor unit.

14. A computer data signal embodied in a carrier wave and representing a sequence of instructions which, when executed by a processor, cause the processor to perform a method of controlling computation in a computer system which includes a plurality of memory banks, the method comprising the steps of:

instructing, at a processor unit, additional processing units each of which is connected to one of the memory banks and works independent of the processor unit, to perform an operation;

reading, at the additional processing unit, data located in an address designated by the processor unit from the corresponding memory bank;

performing, at the additional processing unit, the operation instructed by the processor unit about the read data; and

writing, at the additional processing unit, the result of the operation into the address designated by the processor unit.